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09/960,630	09/20/2001	John Erik Lindholm	NVIDP055/P000369	4492

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EXAMINER	
QUILLEN, ALLEN E	
ART UNIT	**PAPER NUMBER**
2676	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/960,630	Applicant(s) LINDHOLM ET AL.
	Examiner Allen E. Quillen	Art Unit 2676

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 02 September 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-53 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-53 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Double Patenting

1. Claims 1, 13-15, 19-21, 51-52 were provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-34 of copending Application No. 09/885,382. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented. Therefore, the terminal disclaimer is received and added to the record.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 11, 13-15, 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for in the use of the term "swizzle", failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term is not defined within the claims or the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-13, 15-22, 26, 30-34, 37, 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Read, U.S. Patent 5,689,695 and Duluk, et al, U.S. Patent 6,597,363.

8. Regarding claim 1, representative of claims 13, 15-17, 19-22, 26, 30-34, 51-52, as best understood by the Examiner, Read discloses a method for branching during programmable processing in a computer graphics pipeline (Column 4, lines 42-46, 58-65; Column 5, lines 22-28; Figure 49, (found on Sheet 28 of 37), Column 8, lines 40-43), comprising: (a) receiving data (*data input,* Figures 10a-10c, Column 6, lines 33-40; Column 29, lines 39-54) (*floating point format*, Column 12, line 30); (b) performing [claim 22, mathematical] programmable operations

on the data in order to generate output (Figure 10d), wherein the operations are programmable by a user (*a document scanner,* Column 9, lines, 18, 61; Column 13, lines 53-56; Column 67, lines 4-20) utilizing instructions from a predetermined instruction set (Table 1, Column 18, lines 5-40) (c) branching between the programmable operations in a programmable manner (Column 13, lines 50-51; Column 62, lines 7-8); and (d) storing the output in memory (Column 9, lines 22-28), wherein a swizzle (*persistent memory*, pointers, Column 81, lines 33-46) operation is performed; a source buffer for storing data (Column 168, lines 17-36); in one cycle in the computer graphics pipeline (Claim 30) (Column 15, lines 44-48).

Read does not disclose storing using [*vector*, page 19, lines 10-12] component re-mapping. Duluk teaches component re-mapping (Columns 91-104; *interpolate the unit vector components*, Column 98, lines 15-21; *memory caching schemes,* Column 103, lines 20-41). The motivation for combining graphics pipeline programmable operations with vector component re-mapping is for better visual results (Column 98, lines 18-20) when using 3D application program interfaces (API's) such as OpenGL and D3D (Column 6, lines 30-41; Column 14, lines 3-63). Duluk is evidence that at the time of the invention it would have been obvious to combine the benefits of programmable operations in a graphics pipeline, as Read discloses, with vector component operations, as Duluk teaches, for better visual results when using 3D application program interfaces (API's) such as OpenGL and D3D.

Read does not disclose [further, Claims 22, 31-33] wherein the mathematical function is a function in which an initial n derivatives are capable of being tabulated and accessed via an interpolation operation. Duluk teaches wherein the mathematical function is a function in which an initial *n* derivatives are capable of being tabulated and accessed via an interpolation

operation (*tan, cos, sin, triangle descriptors,* Column 78, line 60 through Column 79, line 67; see above, *barycentric interpolation for triangles,* Column 97-99). The motivation for combining graphics pipeline programmable operations with derivative-based interpolation operation is for better visual results (Column 98, lines 18-20) when using 3D application program interfaces (API's) such as OpenGL and D3D (Column 6, lines 30-41; Column 14, lines 3-63). Duluk is evidence that at the time of the invention it would have been obvious to combine the benefits of programmable operations in a graphics pipeline, as Read discloses, with derivative-based interpolation operation, as Duluk teaches, for better visual results when using 3D application program interfaces (API's) such as OpenGL and D3D.

Read does not disclose [further, claims 34, 51-52] method for executing a function, identifying the function to be executed on the input data; preprocessing the input data based on the function to be executed on the input data; processing the input data utilizing a plurality of operations independent of the function to be executed on the input data. Duluk discloses method for executing a function, identifying the function to be executed on the input data (*OpenGL pixel ownership tests,* Columns 7-8; *logicop*); preprocessing the input data based on the function to be executed on the input data; processing the input data utilizing a plurality of operations independent of the function to be executed on the input data (*pipeline state, change on a per-vertex basis*, Columns 5-6). The motivation for combining graphics pipeline programmable operations with conditional functional processing is for better visual results (Column 98, lines 18-20) when using 3D application program interfaces (API's) such as OpenGL and D3D (Column 6, lines 30-41; Column 14, lines 3-63). Duluk is evidence that at the time of the invention it would have been obvious to combine the benefits of programmable operations in a

graphics pipeline, as Read discloses, with conditional functional processing, as Duluk teaches, for better visual results when using 3D application program interfaces (API's) such as OpenGL and D3D.

9. Regarding claim 2, representative of claims 3-6, Read discloses a method as recited in claim 1, wherein the programmable operations are branched to labels (Column 145, line 11), wherein the labels are stored in a table and the programmable operations are branched to indexes in the table (Table 58, index register, Column 143, lines 25-35), each index is stored in an address register (Column 142, line 66 through Column 143, line 20), each index is calculated (Column 143, line 48).

10. Regarding claim 7, Read discloses a method as recited in claim 1, and further comprising terminating the programmable operations after a predetermined number of operations have been performed (Column 162, line 16; Column 166, lines 56-62).

11. Regarding claim 8, representative of claims 9-10, Read discloses a method as recited in claim 1, wherein the programmable operations are branched based on condition codes (*mnemonic*), wherein the condition codes are sourced as EQ(equal), NE(not equal), LT(less), GE(greater or equal), LE(less or equal), GT(greater), FL(false), and TR(true) (Column 115, lines 26-60; Column 117, lines 59-61), wherein the condition codes are maskable (Column 21, lines 21-58; Table 17).

12. Regarding claim 11, as best understood by the examiner, Read discloses a method as recited in claim 8, wherein the condition codes are swizzled (*persistent memory*, pointers, Column 81, lines 33-46).

Read does not disclose using [*vector*, page 19, lines 10-12] component re-mapping. Duluk teaches component re-mapping (Columns 91-104; *interpolate the unit vector components*, Column 98, lines 15-21; *memory caching schemes,* Column 103, lines 20-41). The motivation for combining graphics pipeline programmable operations with vector component re-mapping is for better visual results (Column 98, lines 18-20) when using 3D application program interfaces (API's) such as OpenGL and D3D (Column 6, lines 30-41; Column 14, lines 3-63). Duluk is evidence that at the time of the invention it would have been obvious to combine the benefits of programmable operations in a graphics pipeline, as Read discloses, with vector component operations, as Duluk teaches, for better visual results when using 3D application program interfaces (API's) such as OpenGL and D3D.

13. Regarding claim 12, representative of claim 21, Read discloses a method as recited in claim 1, wherein the operations are selected from the group consisting of a branch operation (Column 62, lines 7-9; Column 89, lines 14-40), call operation (Column 90, line 18), a return operation, a cosine operation (Column 146, line 3), a sine operation, a floor operation, a fraction operation, a set-on-equal operation, a set false operation, a set-on-greater-than, a set-on-less-than-or-equal operation, a set-on-not-equal-to- operation, a set true operation, a no operation, address register load, move (Abstract), multiply, addition, multiply and addition, reciprocal, reciprocal square root, three component dot product, four component dot product, distance

vector, minimum, maximum (Column 152, lines 51), set on less than, set on greater or equal than, exponential base two (2), logarithm base two (2), exponential, logarithm, and/**or** light coefficients (Column 15, lines 25-60; Column 18, line 67, Column 19, line 5, Table 41, Column 115; Column 21, lines 21-58; *branch...pipeline*, Column 94, lines 19-38; *graphics processor*, Column 108, lines 48-49).

14. Regarding claim 18, Read discloses a method as recited in claim 17, wherein the write masks are controlled utilizing an AND operation (see above, Column 5, lines 40-44).

15. Regarding claim 37, Read discloses a method as recited in claim 34, wherein the pre-processing includes performing a conditional 1's complement operation on the input data if the function to be executed on the input data is at least one of sine or cosine (Column 61, lines 21-22; Column 146, line 3).

Claim Rejections - 35 USC § 103

16. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Read, U.S. Patent 5,689,695 and Duluk, et al, U.S. Patent 6,597,363 as applied to claim 1 above, and further in view of Deering, U.S. Patent 5,517,611.

17. Regarding claim 14, Read discloses a system for branching during programmable [graphics] processing (see above, Column 4, lines 42-46) comprising: (a) a source buffer for storing data; (b) a functional module (Figure 54 element 101, Column 167, lines 45-67) coupled to the source buffer for performing programmable operations on the data received therefrom in

order to generate output, wherein the operations are programmable by a user utilizing instructions form a predetermined instruction set; and (c) a register coupled to the functional module for storing the output (Abstract; Column 4, line 52); (d) wherein functional module is capable of branching between the programmable operations (see above); wherein a swizzle (*persistent memory*, pointers, Column 81, lines 33-46) operation is performed.

Read does not disclose vertex processing. Deering teaches vertex processing (Column 1, lines 42-49) in graphics accelerator digital signal processing. The motivation for combining a conditional graphics pipeline using branch conditions with vertex graphics processing is to improve graphics performance while minimizing accelerator costs (Column 1, lines 58-63). Deering is evidence that at the time of the invention it would have been obvious to one skilled in the art of graphics processing to combine the benefits of a conditional graphics pipeline using image processing, as Read discloses, with graphics vertex processing, as Deering teaches, to achieve improved graphics performance while using graphics accelerator in digital signal processing.

Read does not disclose using [*vector*, page 19, lines 10-12] component re-mapping. Duluk teaches component re-mapping (Columns 91-104; *interpolate the unit vector components*, Column 98, lines 15-21; *memory caching schemes,* Column 103, lines 20-41). The motivation for combining graphics pipeline programmable operations with vector component re-mapping is for better visual results (Column 98, lines 18-20) when using 3D application program interfaces (API's) such as OpenGL and D3D (Column 6, lines 30-41; Column 14, lines 3-63). Duluk is evidence that at the time of the invention it would have been obvious to combine the benefits of programmable operations in a graphics pipeline, as Read discloses, with vector component

operations, as Duluk teaches, for better visual results when using 3D application program interfaces (API's) such as OpenGL and D3D.

Claim Rejections - 35 USC § 103

18. Claims 23-25, 27-29, 35-36, 38-50 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Read, U.S. Patent 5,689,695 and Duluk, et al, U.S. Patent 6,597,363 as applied to claims 1, 22 and 34 above, and further in view of Choe, et al, U.S. Patent 6,385,632.

19. Regarding claim 23, representative of claims 24-25, 27-29, 35-36, 38-50 and 53, Read discloses a method of claims 1 and 22, (see above) wherein a computer graphics pipeline using mathematical functions of cosine.

Read does not disclose sine, tangent, arctangent, logarithm, hyperbolic cosine (Claims 23-24); initial n derivatives (Claim 25); Taylor series (Claim 27); cordic algorithm (Claim 28); first and second coordinate system (Claim 29). Choe teaches sine, tangent, arctangent, logarithm, hyperbolic cosine (Claims 23-24); initial *n* derivatives (Claim 25); Taylor series (Claim 27); cordic algorithm (Claim 28); first and second coordinate system (Column 1, lines 8-22; Column 8, lines 30-37, 66; Column 16, lines 19-26; 34-50; Column 3, lines 1-5; Column 15, lines 66-67; Column 17, lines 45-48). The motivation for combining a conditional graphics pipeline using branch conditions with these functions and the cordic algorithm is that they can be computed via the algorithm in significantly less time than direct computations using a plurality of stages, that is in a 3D graphics pipeline generating rotations (Column 15, lines 32-43; Column 2, lines 55-67; Column 4, lines 52-61). Choe is evidence that at the time of the invention it

would have been obvious to one skilled in the art of pipeline processing to combine the benefits of a conditional graphics pipeline using branch conditions, as Read discloses, with the cordic algorithm and these mathematical functions, as Choe teaches, to enable faster processing.

Read does not disclose [further, Claim 53] wherein the mathematical function is a function in which an initial n derivatives are capable of being tabulated and accessed via an interpolation operation. Duluk teaches wherein the mathematical function is a function in which an initial *n* derivatives are capable of being tabulated and accessed via an interpolation operation (*tan, cos, sin, triangle descriptors,* Column 78, line 60 through Column 79, line 67; see above, *barycentric interpolation for triangles,* Column 97-99). The motivation for combining graphics pipeline programmable operations with derivative-based interpolation operation is for better visual results (Column 98, lines 18-20) when using 3D application program interfaces (API's) such as OpenGL and D3D (Column 6, lines 30-41; Column 14, lines 3-63). Duluk is evidence that at the time of the invention it would have been obvious to combine the benefits of programmable operations in a graphics pipeline, as Read discloses, with derivative-based interpolation operation, as Duluk teaches, for better visual results when using 3D application program interfaces (API's) such as OpenGL and D3D.

Response to Arguments

20. Applicant's arguments with respect to claims 1-53 have been considered but are moot in view of the new ground(s) of rejection.

21. The Applicant states "Read….fails to disclose…"swizzle operation."" (Page 13, last two paragraphs).

22. The Examiner respectively notes, however, that (1) Applicant no where defines the term "swizzle" with specificity, (2) Read does disclose one meaning of a term "swizzle" which is persistent memory of objects using memory pointers (Column 81, lines 33-46). The objects can be primitives such as triangles or fragments created and stored for retrieval speed.

23. The Applicant states "that the Examiner has not specifically addressed Claim 21" (Page 14, second paragraph from the top).

24. The Examiner respectfully agrees (see paragraphs 8 and 13 above). The phrase "representative of claim 21" was mistakenly left out of the claim 12 rejection.

25. The Applicant states "that the Examiner has not specifically addressed Claim 21 with at least ten (10)…[features found in] claim 12…[for a] 'computer graphics pipeline' [using] programmable operations" (Page 14, paragraphs 1-3).

26. The Examiner respectfully notes, however, that Read does disclose (1) at least 10 of the branch condition features as cited; (2) a graphics pipeline branching scheme using mathematical logic, (3) user utilizing instructions from a predetermined instruction set (*a document scanner,* Column 9, lines, 18, 61; Column 13, lines 53-56; Column 67, lines 4-20) to generate output. Furthermore, Duluk teaches a programmable graphics pipeline application program to interface with *OpenGL*@ extensions (*a programmer,* Column 5, lines 1-5; Column 6, lines 34-35).

27. The Applicant states "that the Examiner has not addressed the subject matter of Claims 34, and 51-52." (Page 14, last paragraph).

28. The Examiner respectfully agrees and has found another reference. Duluk discloses method for executing a function, identifying the function to be executed on the input data (*OpenGL pixel ownership tests,* Columns 7-8; *logicop*); preprocessing the input data based on the function to be executed on the input data; processing the input data utilizing a plurality of operations independent of the function to be executed on the input data (*pipeline state, change on a per-vertex basis*, Columns 5-6).

29. The Applicant argues that "claims 22, 31-33 to include subject matter of claim 25" (Page 15, third paragraph).

30. The Examiner agrees and has found another reference. Duluk teaches wherein the mathematical function is a function in which an initial *n* derivatives are capable of being tabulated and accessed via an interpolation operation (*tan, cos, sin, triangle descriptors,* Column 78, line 60 through Column 79, line 67; see above, *barycentric interpolation for triangles,* Column 97-99).

31. The Applicant states that "that the Examiner has not addressed the subject matter of Claims 53…" (Page 15, last paragraph).

32. The Examiner respectfully agrees and has found another reference. The Examiner has combined the references Read, Duluk and Choe which together teach all the features of Claim 53.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

***October 28, 2003

Matthew C. Bella

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